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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SATOSHI IKEDA

Appeal 2008-3119
Application 10/052,736[1]
Technology Center 2100

Decided: November 20, 2008

Before HOWARD B. BLANKENSHIP, JAY P. LUCAS, and THU A. DANG, *Administrative Patent Judges*.

LUCAS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF CASE

Appellant appeals from a twice rejection of claims 6 to 32 under authority of 35 U.S.C. § 134(a). The Board of Patent Appeals and

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[1] Application filed January 23, 2002. Appellant claims the benefit under 35 U.S.C. § 119 of Japan application P2001-015332, filed 01/24/2001. The real party in interest is Sony Corporation of Tokyo, Japan.

Interferences (BPAI) has jurisdiction under 35 U.S.C. § 6(b). Claims 1 to 5 are canceled.

Appellant's invention relates to a semiconductor testing method and apparatus in which the internal timing (cycle period) is variable, so a wider range of semiconductors can be accommodated. In the words of the Appellant:

> Disclosed are semiconductor testing apparatus and method for changing the cycle period of a specific address test pattern in testing a semiconductor device. The semiconductor testing apparatus includes test pattern memory means adapted for storing and managing test pattern data in accordance with addresses, and outputting the test pattern specified by the desired address; test pattern generation means for generating a test pattern signal on the basis of the test pattern outputted from the memory means; and control means for controlling the test pattern memory means and the test pattern generation means in such a manner that the test pattern signal based on the test pattern data of the desired address can be generated at a predetermined timing conforming with the set information.

(Abstract, Spec., 24).

Claim 6 is exemplary:

6. A semiconductor testing apparatus comprising:

control means adapted to generate a timing signal and an address specifying signal, said timing signal having a test pattern cycle period, the duration of said test pattern cycle period being variable, the rate of modification for said address specifying signal being said test pattern cycle period;

test pattern memory means adapted to store a first test pattern, said first test pattern being outputted from said test pattern memory means in response to said address specifying signal, the rate of output for said first test pattern being said test pattern cycle period;

and

test pattern generation means adapted to generate an input test pattern signal by combining said first test pattern with said timing signal, a semiconductor device under test receiving said input test pattern signal.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Reichert	US 6,553,529 B1	Apr. 22, 2003 (filed Jul. 23, 1999)

REJECTION

Claims 6 to 32 stand rejected by the Examiner under 35 U.S.C. § 102(e) for being anticipated by Reichert.

Appellant contends that the claimed subject matter is not anticipated by Reichert, for failure of Reichert to teach claimed limitations. The Examiner contends that each of the claims is properly rejected.

Rather than repeat the arguments of Appellant or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellant have been considered in this opinion. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered and are deemed to be waived.

We affirm the rejection.

ISSUE

The issue is whether Appellant has shown that the Examiner erred in rejecting the claims under 35 U.S.C. § 102(e). The issue turns on whether Reichert teaches the address specifying signal and the test pattern timing signal as claimed, and other specific limitations.

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

1. Appellant invented an apparatus for testing semiconductors (and an associated method) in which the timing can be speeded up or slowed down during various sections of the test. (Spec., 4, middle). Appellant stores test patterns in a memory #130, from which, at the behest of a control signal, called the address specifying signal (since it chooses the proper test signal in memory based on its address), they are joined to a timing signal in device #120 and sent as input to the semiconductor device under test #500. (Spec., 10, middle). Meanwhile, a portion of the test pattern is sent to a decision means #140 to be compared with the output from the semiconductor device, to generate a result. (Spec., 10, bottom).

2. The reference Reichert is also directed to an apparatus and method for testing semiconductor devices. (Col. 4, l. 13+), with the capability of high speed or low speed timing modes related to test patterns requiring the different modes. (Col. 3, ll. 4 to 8). Control means (test controller 22, and timing system 30) combine a test pattern from the pattern generation circuit #24 for testing the semiconductor device with timing data (Col. 4, l. 41*ff)*. The timing logic #34 supports high speed and low speed testing of the Device Under Test #28 (DUT). (Col. 4, l. 49). The global timeset address line 29 couples the pattern generator to the timing system and also to the failure processor 50 via the system bus 26. (Col. 4, l. 31). Thus, the test pattern information is used in the generation of the input test pattern (*id*) combined with the timing signal. (Col. 4, l. 41), and in the analysis of the DUT output.

PRINCIPLES OF LAW

"In reviewing the [E]xaminer's decision on appeal, the Board must necessarily weigh all of the evidence and argument." *In re Oetiker*, 977 F.2d 1443, 1445 (Fed. Cir. 1992).

In rejecting claims under 35 U.S.C. § 102, "[a] single prior art reference that discloses, either expressly or inherently, each limitation of a claim invalidates that claim by anticipation." *Perricone v. Medicis Pharm. Corp.,* 432 F.3d 1368, 1375-76 (Fed. Cir. 2005) (citation omitted).

"Anticipation of a patent claim requires a finding that the claim at issue 'reads on' a prior art reference." *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1346 (Fed Cir. 1999) ("In other words, if granting patent protection on the disputed claim would allow the patentee to exclude the public from practicing the prior art, then that claim is anticipated, regardless of whether it also covers subject matter not in the prior art.") (internal citations omitted).

The analysis begins with an interpretation of the claims: "Both anticipation under § 102 and obviousness under § 103 are two-step inquiries. The first step in both analyses is a proper construction of the claims . . . . The second step in the analyses requires a comparison of the properly construed claim to the prior art." *Medichem S.A. v. Rolabo, S.L.*, 353 F.3d 928, 933 (Fed. Cir. 2003) (internal citations omitted).

ANALYSIS

From our review of the administrative record, we find that Examiner has presented a prima facie case for the rejection of Appellant's claims under 35 U.S.C. § 102. The prima facie case is presented on pages 3 to 6 of the Examiner's Answer. In opposition, Appellant presents a number of arguments.

The claims contain certain limitations which this panel believes to be indefinite. Specifically, in the first clause in claim 6, the expression "…, the rate of modification for said address specifying signal being said test pattern

cycle period" is not clear. For the purposes of reviewing the Examiner's rejection under 35 U.S.C. § 102 we have interpreted that clause in a manner consistent with the disclosure in the Specification, as will be evident below. However, we have also rejected the claims under 35 U.S.C. § 112, ¶ 2 for being unclear in a separate section of this opinion.

Arguments with respect to the rejection of claims 6 to 32 under 35 U.S.C. § 102

Appellant contends that Examiner erred in rejecting claim 6 for failure of Reichert to disclose "***the pattern generation circuit 24 as being adapted to output a first test pattern in response to an address specifying signal generated by the control means, wherein the rate of output for the first test pattern is the test pattern cycle period.***" (App. Br., 12, middle).

Claim 6 is expressed in means plus function terms, and thus the Appellant's reference to a specific item (e.g., circuit 24) may be misleading when the same function is provided by a number of different items in the reference. Though the Examiner points out that workstation 22 of Reichert operates as a test controller, the reference Reichert need only teach or suggest that one or more devices ("means") perform the stated function. The function need not be embodied in a single device of Reichert.

Appellant's contention relates to the second clause of the claim, starting with the phrase "test pattern memory means…." As noted in FF#2 above, Reichert teaches that test patterns generated by #24 and sent to timing

memory #38 (Col. 4, l. 32) are outputted in accordance with control signals from, *inter alia*, Test Controller #22. The Examiner has read the signals outputting the proper patterns from the memory #38 as the claimed address specifying signal. (Answer, 7, top). In the claims, the function of the address specifying signal is stated to cause "said first test pattern [to be] outputted from said test pattern memory means." As the said control signals in Reichert function as specified in the claim we do not find error in the Examiner's analysis.

Appellant next argues that Reichert fails to teach the test controller 22 as being adapted to output a first test pattern in response to an address specifying signal. (App. Br., 12, bottom). As we mentioned above, the means plus function language in Claim 6 is broader than the Appellant's argument. The claim only requires a "first test pattern being outputted from said test pattern memory means in response to said address specifying signal." In Reichert, a pattern memory produces test patterns that are fed to the Device Under Test according to a DUT clock period. (Reichert, Col. 3, l. 6). The reference thus anticipates the claim limitation.

Appellant next contends that Reichert fails to disclose a failure processing circuit adapted to detect a failure within the DUT comparing an output test pattern with the first test pattern. (App. Br., 13, middle). In response we note that Reichert teaches the pattern information going "to and from the failure processor [is] distributed via the system bus 26." (Col. 4, ll. 32-34). The failure processor #50 receives the output of the DUT. (Fig. 1).

Appellant's arguments concerning the dependent claims and the parallel method claims are considered to be answered by the Examiner, in consideration of the teachings of Reichert.

Rejection
of claims 6 to 32
under 35 U.S.C. § 112, ¶ 2

We make the following new grounds of rejection using our authority under 37 C.F.R. § 41.50(b).

Rejection:

Claims 6 to 32 are rejected under 35 U.S.C. § 112 ¶ 2 for being unclear.

Each of the claims contains a clause "**the rate of modification for said address specifying signal being said test pattern cycle period.**" We find this clause unclear, as the definition of the rate of modification for the test pattern cycle period has not been adequately presented. In the Appeal Brief, the definition of the test pattern cycle period refers to the Specification, at Figures 2 through 4. (App. Br., 3, middle). The figures indicate charts with a time abscissa, which is consistent with the standard definition of a cycle period. A rate of modification would be a ratio of times, as, for example, 6 microseconds per millisecond. That rate of modification would be expressed as a whole number (e.g., 2 times or 3 times) or a time (for the modification) per a unit of time. However, that is

not internally consistent with the stated rate of modification being a cycle period, in the questionable clause.

For the sake of the rejection under 35 U.S.C. § 102 we have interpreted the address specifying signal as functionally defined in the claims, namely as the cause of the first test pattern being outputted from the test pattern memory. We have also interpreted the test pattern cycle period as expressed in the claims, namely the period of a portion of the test pattern. However, we have not interpreted the whole phrase in question, for lack of understandable clarity.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that the Examiner did not err in rejecting claims 6 to 32. We also conclude that the same claims are unclear.

DECISION

The rejection of claims 6 to 32 under 35 U.S.C. § 102 is affirmed.

Claims 6 to 32 stand rejected under 35 U.S.C. § 112, ¶ 2.

We have sustained the Examiner's prior art rejection with respect to claims 6 to 32, all the claims on appeal. Moreover, we have entered a new ground of rejection under 37 C.F.R. § 41.50(b) for claims 6 to 32 for being unclear under 35 U.S.C. § 112 ¶ 2.

With respect to the affirmed rejection(s), 37 C.F.R. § 41.52(a)(1) provides that "Appellant may file a single request for rehearing within two months from the date of the original decision of the Board."

In addition to affirming the Examiner's rejection(s) of one or more claims, this decision contains a new ground of rejection pursuant to 37 C.F.R. § 41.50(b). 37 C.F.R. § 41.50(b) provides that "[a] new ground of rejection pursuant to this paragraph shall not be considered final for judicial review."

37 C.F.R. § 41.50(b) also provides that the Appellant, WITHIN TWO MONTHS FROM THE DATE OF THE DECISION, must exercise one of the following two options with respect to the new ground of rejection to avoid termination of the appeal as to the rejected claims:

> (1) *Reopen prosecution.* Submit an appropriate amendment of the claims so rejected or new evidence relating to the claims so rejected, or both, and have the matter reconsidered by the examiner, in which event the proceeding will be remanded to the examiner. . . .
>
> (2) *Request rehearing.* Request that the proceeding be reheard under § 41.52 by the Board upon the same record. . . .

Should Appellant elect to prosecute further before the Examiner pursuant to 37 C.F.R. § 41.50(b)(1), in order to preserve the right to seek review under 35 U.S.C. §§ 141 or 145 with respect to the affirmed rejection, the effective date of the affirmance is deferred until conclusion of the

prosecution before the Examiner unless, as a mere incident to the limited prosecution, the affirmed rejection is overcome.

If Appellant elects prosecution before the Examiner and this does not result in allowance of the application, abandonment or a second appeal, this case should be returned to the Board of Patent Appeals and Interferences for final action on the affirmed rejection, including any timely request for rehearing thereof.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

37 C.F.R. § 41.50(b)

rwk

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